

Contents

Abstract	v
Zusammenfassung	vii
Contents	ix
1 Introduction	1
1.1 Recent Trends in Mobile Communications	3
1.2 Contributions	5
1.3 Outline of the Thesis	6
2 Design Space Exploration	7
2.1 Terminology	8
2.2 High-level criteria for complexity	9
2.3 Implementation-related Algorithm Characteristics	10
2.3.1 Numerical Properties and Operations	11
2.3.2 Storage and Bandwidth	12
2.3.3 Structure and Timing	16
2.3.4 Reliable Algorithm Complexity Specifications	18
2.3.5 Summary	19
2.4 Metrics for comparing Architecture Complexity	19
2.4.1 Implementation Complexity Metrics	20
2.4.2 Technology Scaling	21
2.5 Evaluation of Hardware Platforms	26
2.5.1 On the Suitability of Processors and ASICs	27

2.5.2	Signal Processing in Wireless Communications	31
2.6	Digital Design for Low Power	35
2.6.1	Power and Energy in CMOS Circuits	36
2.6.2	Principles of Energy-Efficient ASIC Design	39
2.7	Summary	43
3	Turbo Decoder Design and Optimization	45
3.1	Turbo Coding	46
3.1.1	3GPP Turbo Encoder	46
3.1.2	The Turbo Decoding Algorithm	48
3.1.3	Extrinsic Scaling	49
3.2	High-Level Architecture Exploration	50
3.2.1	Interleaver and Block Size	52
3.2.2	High-Level Architecture Efficiency	53
3.2.3	Memory Bandwidth Bottleneck	56
3.2.4	Architectures for HSDPA and LTE	57
3.3	Optimized SISO Decoder Design	60
3.3.1	The SISO Decoding Algorithm	60
3.3.2	Max-log-MAP Decoder Core	64
3.3.3	Low-Complexity Radix-2 ACS Unit	68
3.3.4	Radix-2 versus Radix-4	74
3.3.5	Summary	77
3.4	Implementation of a 3GPP Interleaver	77
3.4.1	HSDPA Interleaver	78
3.4.2	Summary and Comparison	84
3.5	Turbo Decoder Implementations	84
3.5.1	Low-Power HSDPA Turbo Decoder	85
3.5.2	Turbo Decoder for EGPRS-2	86
3.5.3	Turbo Decoder for HSDPA+	88
3.5.4	Turbo Decoder for 3GPP LTE	89
3.6	Summary	90
4	Digital Receiver Design for the GSM Evolution	93
4.1	System Overview	94
4.2	Equalizer Concepts for EGPRS	98
4.2.1	Linear Equalizer	99
4.2.2	Maximum Likelihood Sequence Estimator	100
4.2.3	Delayed Decision Feedback Sequence Estimator	101

4.2.4	Turbo Equalizers	104
4.3	Exploration of Channel Equalization	107
4.3.1	Characterization of DDFSE	107
4.3.2	Pre-Filtering with Minimum-Phase Filter	109
4.3.3	Length of DDFSE History	112
4.3.4	Summary	113
4.4	Low-Complexity Pre-filter	114
4.4.1	Pre-filter Concept	115
4.4.2	Modified Levinson-Durbin Algorithm	117
4.4.3	Sequential Pre-filter Implementation	121
4.4.4	Summary	124
4.5	Efficient DDFSE Implementation	124
4.5.1	Branch Metric Generation	125
4.5.2	Parallelization in DDFSE Implementations	128
4.5.3	Summary	135
4.6	VLSI Implementations and Comparison	136
4.6.1	Digital Receiver ASICs Overview	137
4.6.2	Receiver Performance	139
4.6.3	Discussion and Comparison	140
4.7	Summary	146
5	Summary and Conclusion	149
A	Chip photos	155
B	GSM Test Channels	159
C	GSM Pulses	163
	Acronyms	165
	Bibliography	167
	Curriculum Vitae	177